# Power MOSFET 20 V, 5.6 A Single N-Channel, TSOP-6

#### **Features**

- Leading Edge Trench Technology for Low On Resistance
- Low Gate Charge for Fast Switching
- Small Size (3 x 2.75 mm) TSOP-6 Package
- This is a Pb-Free Device

#### **Applications**

- DC-DC Converters
- Lithium Ion Battery Applications
- Load/Power Switching

# **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit			
Drain-to-Source Voltage			V <sub>DSS</sub>	20	V	
Gate-to-Source Voltage			V <sub>GS</sub>	±8	V	
	Steady	T <sub>A</sub> = 25°C		5.6		
Continuous Drain Current (Note 1)	State	T <sub>A</sub> = 85°C	I <sub>D</sub>	4.1	А	
,	t ≤ 10 s	T <sub>A</sub> = 25°C		6.2		
Power Dissipation	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.1	W	
(Note 1)	t ≤ 10 s			1.4		
Continuous Drain Current		T <sub>A</sub> = 25°C	,	4.2	А	
(Note 2)	Steady	T <sub>A</sub> = 85°C	I <sub>D</sub>	3.0		
Power Dissipation (Note 2)	State	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.6	W	
Pulsed Drain Current	I <sub>DM</sub>	19	Α			
Operating and Storage Ten	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C			
Source Current (Body Diod	IS	1.0	Α			
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C	

# THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)		110	
Junction-to-Ambient - t ≤ 10 s (Note 1)	$R_{\theta JA}$	90	°C/W
Junction-to-Ambient - Steady State (Note 2)		200	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
- 2. Surface-mounted on FR4 board using the minimum recommended pad size

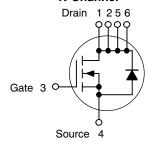


# ON Semiconductor®

#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> mAX	I <sub>D</sub> Max	
20 V	24 mΩ @ 4.5 V	5.6 A	
	32 mΩ @ 2.5 V	4.9 A	

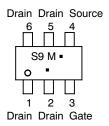
### **N-Channel**



# MARKING DIAGRAM & PIN ASSIGNMENT



TSOP-6 CASE 318G STYLE 1



S9 = Specific Device Code

M = Date Code\*

= Pb-Free Package
 (Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>		
NTGS3130NT1G	TSOP-6 (Pb-Free)	3000/Tape & Reel		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** ( $T_C = 25$ °C unless otherwise noted)

Characteristic	Symbol	Test Co	ndition	Min	Тур	Max	Unit	
OFF CHARACTERISTICS					I		I	
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V; I	l <sub>D</sub> = 250 μA	20			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				9.8		mV/°C	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V; \ T <sub>J</sub> = 2	/ <sub>DS</sub> = 16 V, 25°C			1.0	μА	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0, V	′ <sub>GS</sub> = ±8 V			100	nA	
ON CHARACTERISTICS (Note 3)								
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}$	I <sub>D</sub> = 250 μA	0.4	0.6	1.4	V	
Negative Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				3.4		mV/°C	
Desire to Occurre On Besistance		V <sub>GS</sub> = 4.5 V	<sup>7</sup> , I <sub>D</sub> = 5.6 A		19	24		
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 2.5 V	<sup>7</sup> , I <sub>D</sub> = 4.9 A		25	32	mΩ	
Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 10 V	, I <sub>D</sub> = 5.6 A		8.2		S	
CHARGES, CAPACITANCE, & GATE RESIS	TANCE							
Input Capacitance	C <sub>ISS</sub>	V	0.1/		935			
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = f = 1	MHz,		169		pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>	$V_{DS} =$	: 16 V		104			
Input Capacitance	C <sub>ISS</sub>	V	0.1/		965			
Output Capacitance	Coss	V <sub>GS</sub> = f = 1	MHz,		198			
Reverse Transfer Capacitance	C <sub>RSS</sub>	$V_{DS} =$	: 10 V		110			
Total Gate Charge	Q <sub>G(TOT)</sub>				13.2	20.3		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> =			0.60		nC	
Gate-to-Source Charge	Q <sub>GS</sub>	V <sub>DS</sub> = I <sub>D</sub> = 5	5.6 A		1.5			
Gate-to-Drain Charge	Q <sub>GD</sub>				4.2			
Total Gate Charge	Q <sub>G(TOT)</sub>				11.8	18.0		
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> =	4.5 V		0.6			
Gate-to-Source Charge	Q <sub>GS</sub>	$V_{DS} = I_{D} = 0$	6.2 A		1.4			
Gate-to-Drain Charge	Q <sub>GD</sub>				2.7		7	
SWITCHING CHARACTERISTICS, V <sub>GS</sub> = 4.5	<b>5 V</b> (Note 4)			-	•			
Turn-On Delay Time	t <sub>d(ON)</sub>				6.3	12.6		
Rise Time	t <sub>r</sub>	$\begin{array}{c} V_{GS}=4.5 \text{ V,} \\ V_{DD}=16 \text{ V,} \\ I_{D}=1 \text{ A,} \\ R_{G}=3 \Omega \end{array}$			7.3	13.5	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>				21.7	35.1		
Fall Time	t <sub>f</sub>				9.7	17.6		
DRAIN-SOURCE DIODE CHARACTERISTIC	cs			•			· •	
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.0 A	T <sub>J</sub> = 25°C		0.7	1.2	V	
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ Vdc},$ $dI_{SD}/dt = 100 \text{ A}/\mu\text{s},$ $I_{S} = 1.0 \text{ A}$			20.4			
Charge Time	t <sub>a</sub>				8.1		ns	
Discharge Time	t <sub>b</sub>				11.6			
Reverse Recovery Charge	Q <sub>RR</sub>				8.8		nC	

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperature.

### **TYPICAL CHARACTERISTICS**

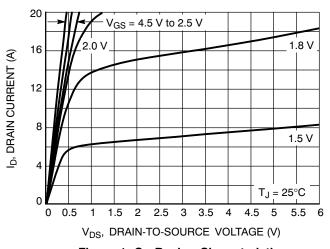


Figure 1. On-Region Characteristics

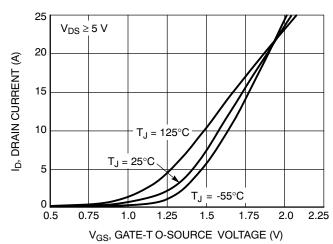


Figure 2. Transfer Characteristics

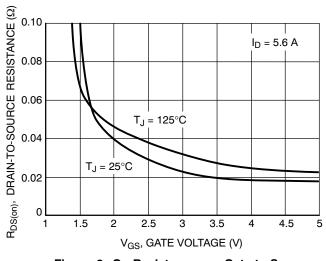


Figure 3. On-Resistance vs. Gate-to-Source Voltage

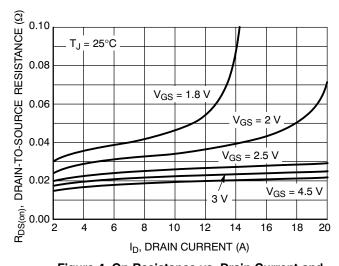


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

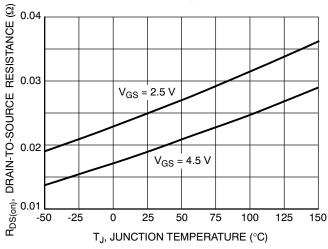


Figure 5. On-Resistance Variation with Temperature

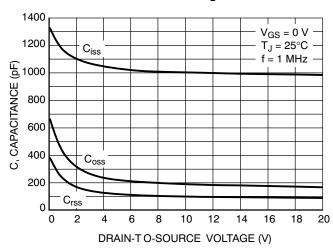


Figure 6. Capacitance Variation

### **TYPICAL CHARACTERISTICS**

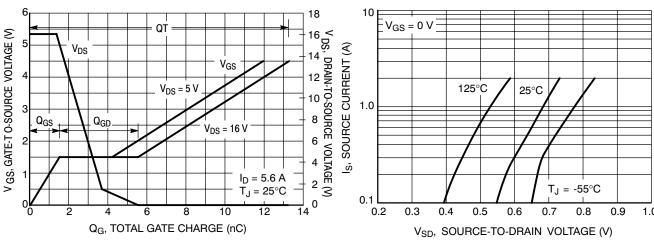


Figure 7. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

Figure 8. Diode Forward Voltage vs. Current

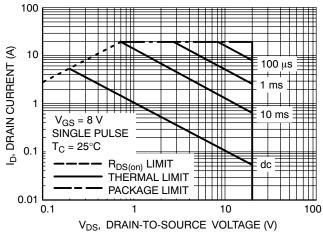


Figure 9. Maximum Rated Forward Biased Safe Operating Area

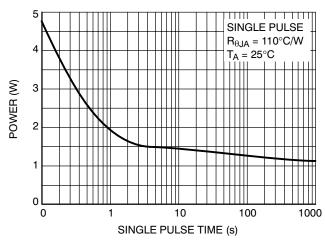


Figure 10. Single Pulse Maximum Power Dissipation

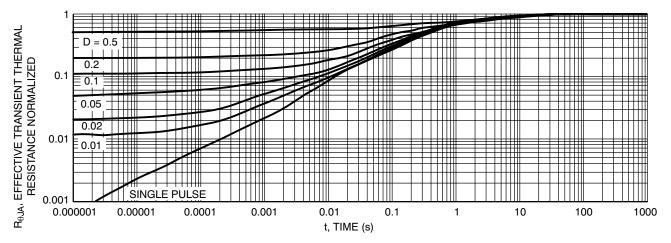
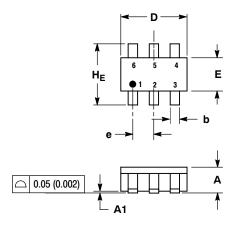
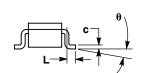


Figure 11. Thermal Response

# PACKAGE DIMENSIONS

### TSOP-6 CASE 318G-02 ISSUE S





#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
   CONTROLLING DIMENSION: MILLIMETER.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH,
- PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
С	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
е	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

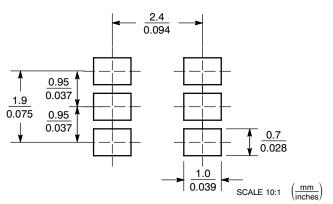
STYLE 1:

- PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE

  - DRAIN

  - 6 DRAIN

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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